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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,137	10/14/2003	Koray Oner	BP 3255.2	4503

34399 7590 03/18/2008
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EXAMINER	
PATEL, JAY P	
ART UNIT	PAPER NUMBER
2619	
MAIL DATE	DELIVERY MODE
03/18/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/685,137	ONER, KORAY	
	Examiner	Art Unit	
	JAY P. PATEL	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7 and 10-19* is/are rejected.

7)☒ Claim(s) *3,6,8,9 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/14/2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. In regards to claims 4 and 19, the terms "N" and "2N" are not defined in the claim. For example, is "N" a positive integer greater than zero? Otherwise, the respective widths would be zero or negative.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1, 2, 5, 7 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weng et al. (US Patent 7012926 B2) in view of Hazama (US Patent 7272147 B2).

3. In regards to claim 1, Weng shows in figure 3, a schematic diagram depicting mapping between a descriptor and a packet buffer.

Figure 4, is a flow diagram showing the procedural steps carried out by the packet receiving-transmitting method in Weng. In the initial step 150, the procedure is

started in response to a received packet (a first interface circuit for receiving packet data on a first channel).

Referring back to figure 3, data buffers 220 read on a memory.

In further regards data buffers 220 are used for storing the packet and descriptors 210 are used for recording related information for the packet and the data buffer such as, an initial address and status of the data buffer, an interrupt information and packet length (a packet manager circuit coupled between the first interface circuit and the memory to receive data on the first channel from the first interface circuit, wherein the packet manager circuit is configured to write at least a first data packet fragment to the memory under control of a first descriptor, and is configured to write at least a second data packet fragment to the memory under control of a second descriptor) (column 6, lines 22-26).

In further regards, when an early receiving interrupt signal is received, the network driving software starts to ***read*** the packet data that has already been stored in the data buffer. When the link layer controller has completely moved the whole packet to the data buffer, an interrupt OK signal is asserted. In the same time, the link layer controller performs a ***write*** back process for reset the descriptor 210 (column 5, lines 3-9) (a controller for controlling descriptor wire back operations to memory in either read-modify-write mode). Furthermore, figure 2 shows a descriptor data structure, where, when the OWN bit is set to 1, it means that the whole descriptor list 210 and data buffers pointed by the descriptor list 210 are all available to the link layer controller. When the link layer controller completely processes for the packet and a write back

process is done (column 5, lines 28-33) (write-invalidate mode, wherein the controller writes a plurality of descriptors together to memory in a single write-invalidate operation).

In further regards to claim 1, Weng fails to teach, a timer for generating a first time-out signal at a predetermined time after the first descriptor is ready for transfer. Hazama however, teaches the above-mentioned limitation. In figure 1, Hazama shows a packet transfer device inclusive of a timing generator 30 which provides timing signals to a read controller 31, a write controller 33 and a write/read processor 34 amongst other things (see column 2, lines 66-67 and column 3, lines 1-3).

Therefore, it would have been obvious to provide timing signals as taught by Hazama into the descriptor based packet transfer apparatus taught by Weng. The motivation to do so would be to improve time and efficiency of occupying the system bus for the link layer controller reading the descriptor list and performing a status writes back procedure (see Weng column 2, lines 57-61).

In regards to claim 2, when an early receiving interrupt signal is received, the network driving software starts to ***read*** the packet data that has already been stored in the data buffer. When the link layer controller has completely moved the whole packet to the data buffer, an interrupt OK signal is asserted. In the same time, the link layer controller performs a ***write*** back process for reset the descriptor 210 (Weng column 5, lines 3-9).

In regards to claim 5, Weng shows in figure 1, the data buffers 120 for temporary storage.

In regards to claim 7, Weng in combination with Hazama teaches all the limitations of parent claim 1. Weng however fails to teach a timer with memory. Hazama however teaches the above-mentioned limitation. In figure 1, Hazama shows a packet transfer device inclusive of a timing generator 30 which provides timing signals to a read controller 31, a write controller 33 and a write/read processor 34 amongst other things (see column 2, lines 66-67 and column 3, lines 1-3).

Therefore, it would have been obvious to provide timing signals as taught by Hazama into the descriptor based packet transfer apparatus taught by Weng. The motivation to do so would be to improve time and efficiency of occupying the system bus for the link layer controller reading the descriptor list and performing a status writes back procedure (see Weng column 2, lines 57-61).

4. In regards to claim 17, Weng shows in figure 3, a schematic diagram depicting mapping between a descriptor and a packet buffer.

Figure 4, is a flow diagram showing the procedural steps carried out by the packet receiving-transmitting method in Weng. In the initial step 150, the procedure is started in response to a received packet (receiving a first and second packet fragment in an interface circuit).

Referring back to figure 3, data buffers 220 read on a memory.

In further regards data buffers 220 are used for storing the packet and descriptors 210 are used for recording related information for the packet and the data buffer such as, an initial address and status of the data buffer, an interrupt information

and packet length (transmitting the first and second packet fragments from the interface circuit to a memory under control of the first and second descriptors) (column 6, lines 22-26).

Furthermore, figure 2 shows a descriptor data structure, where, when the OWN bit is set to 1, it means that the whole descriptor list 210 and data buffers pointed by the descriptor list 210 are all available to the link layer controller. When the link layer controller completely processes for the packet and a write back process is done (column 5, lines 28-33) (writing the first and second descriptors back to memory together as a write-invalidate command).

In further regards to claim 17, Weng fails to teach, setting a timer to expire a predetermined time interval after the first descriptor for the first packet fragment is released. In figure 1, Hazama shows a packet transfer device inclusive of a timing generator 30 which provides timing signals to a read controller 31, a write controller 33 and a write/read processor 34 amongst other things (see column 2, lines 66-67 and column 3, lines 1-3).

Therefore, it would have been obvious to provide timing signals as taught by Hazama into the descriptor based packet transfer apparatus taught by Weng. The motivation to do so would be to improve time and efficiency of occupying the system bus for the link layer controller reading the descriptor list and performing a status writes back procedure (see Weng column 2, lines 57-61).

In regards to claim 18, when an early receiving interrupt signal is received, the network driving software starts to ***read*** the packet data that has already been stored in

the data buffer. When the link layer controller has completely moved the whole packet to the data buffer, an interrupt OK signal is asserted. In the same time, the link layer controller performs a ***write*** back process for reset the descriptor 210 (Weng column 5, lines 3-9).

5. Claim 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weng et al. (US Patent 7012926 B2) in view of Reid et al. (US Patent 6115776).

6. In regards to claim 10, Weng shows in figure 3, a schematic diagram depicting mapping between a descriptor and a packet buffer.

In further regards data buffers 220 are used for storing the packet and descriptors 210 are used for recording related information for the packet and the data buffer such as, an initial address and status of the data buffer, an interrupt information and packet length (a data transfer controller for managing the direct memory transfer of data on a first channel by releasing one or more descriptors associated with said first channel) (column 6, lines 22-26).

In further regards to claim 10, Weng fails to teach, receiving a time-out pulse for the first channel and delaying release of the descriptor until after receiving the time-out pulse for the first channel. Reid teaches the above-mentioned limitation. Reid teaches that a timer can be reset if a controller detects more packets are queued in the transmit buffer and during "countdown" of the delay time if the controller downloads another packet from transmit buffer (see column 6, lines 54-66).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the timer reset operation as taught by Reid

into the descriptor based packet transfer apparatus taught by Weng. The motivation to do so would be to improve time and efficiency of occupying the system bus for the link layer controller reading the descriptor list and performing a status writes back procedure (see Weng column 2, lines 57-61).

In regards to claim 11, figure 2 shows a descriptor data structure, where, when the OWN bit is set to 1, it means that the whole descriptor list 210 and data buffers pointed by the descriptor list 210 are all available to the link layer controller. When the link layer controller completely processes for the packet and a write back process is done (Weng column 5, lines 28-33).

In regards to claim 12, when an early receiving interrupt signal is received, the network driving software starts to ***read*** the packet data that has already been stored in the data buffer. When the link layer controller has completely moved the whole packet to the data buffer, an interrupt OK signal is asserted. In the same time, the link layer controller performs a ***write*** back process for reset the descriptor 210 (column 5, lines 3-9).

In regards to claim 13, Weng in combination with Reid teaches all the limitations of parent claim 10. Weng however, fails to teach a timer for generating a time-out pulse at a predetermined time interval after a first of the plurality of descriptors is received. Reid teaches the above-mentioned limitation. Reid teaches that a timer can be reset if a controller detects more packets are queued in the transmit buffer and during "countdown" of the delay time if the controller downloads another packet from transmit buffer (see column 6, lines 54-66).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the timer reset operation as taught by Reid into the descriptor based packet transfer apparatus taught by Weng. The motivation to do so would be to improve time and efficiency of occupying the system bus for the link layer controller reading the descriptor list and performing a status writes back procedure (see Weng column 2, lines 57-61).

In regards to claim 14, Weng in combination with Reid teaches all the limitations of parent claims 10 and 13. Weng however, fails to teach the predetermined time interval being programmably selected from a plurality of timer interval values. Reid teaches the above-mentioned limitation. Reid teaches shows a timer 110 containing a first timer 114 and a second timer 115 (see column 6, lines 66-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the timer reset operation as taught by Reid into the descriptor based packet transfer apparatus taught by Weng. The motivation to do so would be to improve time and efficiency of occupying the system bus for the link layer controller reading the descriptor list and performing a status writes back procedure (see Weng column 2, lines 57-61).

In regards to claim 15, Weng shows in figure 3, descriptors 210 and memory 220.

In regards to claim 16, Weng shows in figure 3, descriptors 210 and memory 220.

Conclusion

7. Claims 3, 6, 8-9 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 4 and 19 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY P. PATEL whose telephone number is (571)272-3086. The examiner can normally be reached on M-F 9:00 am - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on (571) 272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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